# LM34930 Evaluation Board

National Semiconductor
Application Note 1848
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## Introduction

The LM34930EVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 5V output over an input range of 8V to 33V. The circuit delivers load currents to 1A, with current limit set at a nominal 1.16A. The board is populated with all components except R5, C9 and C10. These components provide options for managing the output ripple as described later in this document.

The board's specification are:

- Input Voltage: 8V to 33V
- Output Voltage: 5V
- Maximum load current: 1A
- Minimum load current: 0A
- Current Limit: 1.14A to 1.19A
- Measured Efficiency: 92.2% ($V_{IN}$ = 8V, $I_{OUT}$ = 400 mA)
- Nominal Switching Frequency: 1500 kHz
- Size: 2.6 in. x 1.6 in. x 0.5 in

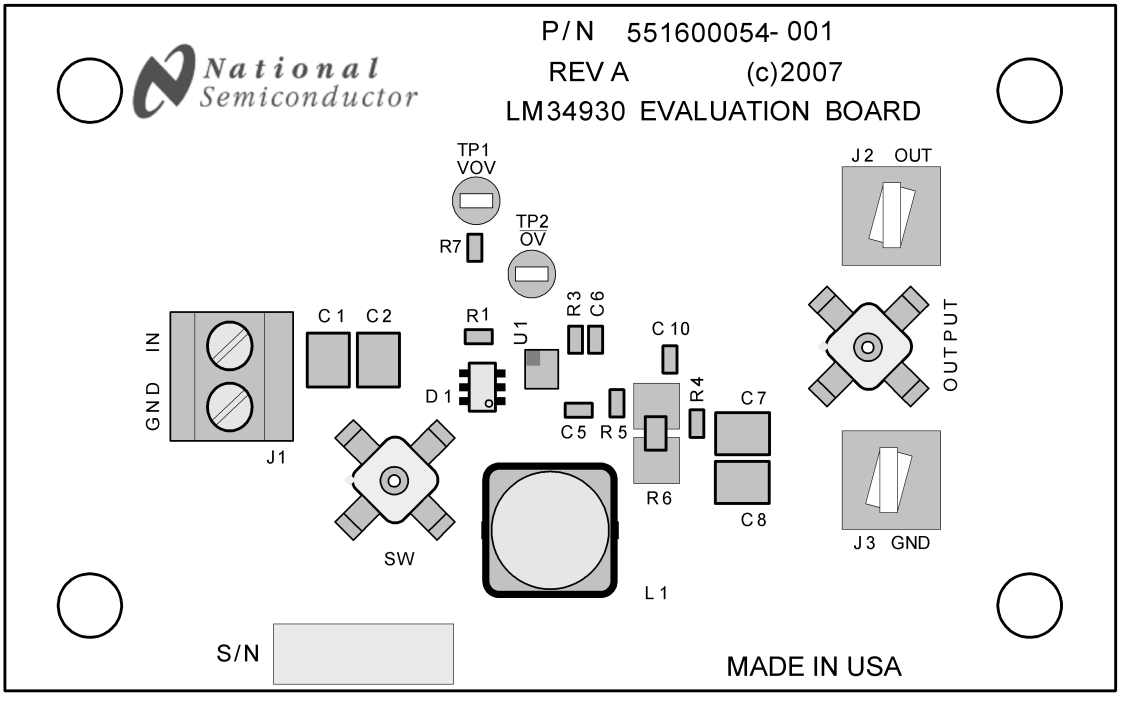



**FIGURE 1. Evaluation Board - Top Side**

## Theory of Operation

Refer to the evaluation board schematic in *Figure 5*. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and VIN according to the equation:

$$t_{ON} = \frac{4.15 \times 10^{-11} \times (R1 + 0.5\ k\Omega)}{V_{IN} - 0.8V} + 65\ ns$$

The on-time of this evaluation board ranges from ≅416 ns at VIN = 8V, to ≅144 ns at VIN = 33V. The on-time varies inversely with VIN to maintain a nearly constant switching frequency. At the end of each on-time the Minimum Off-Timer ensures the buck switch is off for at least 90 ns. In normal operation, the off-time is much longer. During the off-time, the load current is supplied by the output capacitor (C7, C8). When the output voltage falls sufficiently that the voltage at FB is below 2.52V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at FB to switch the regulation comparator. The current limit threshold, is ≅1.19A at Vin = 8V, and ≅1.14A at Vin = 33V. Refer to the LM34930 data sheet for a more detailed block diagram, and a complete description of the various functional blocks.



## Board Layout and Probing

The pictorial in *Figure 1* shows the placement of the circuit components. The following should be kept in mind when the board is powered:

1) When operating at high input voltage and high load current, forced air flow may be necessary.

2) The LM34930, and diode D1 may be hot to the touch when operating at high input voltage and high load current.

3) Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.

4) At maximum load current (1A), the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

## Board Connection/Start-up

The input connections are made to the J1 connector. The load is connected to the J2 (OUT) and J3 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 8V, at which time the output voltage should be 5V. If the output voltage is correct with 8V at VIN, then increase the input voltage as desired and proceed with evaluating the circuit. DO NOT EXCEED 40V AT VIN.

## Output Ripple Control

The LM34930 requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW pin, for proper operation. The required ripple can be supplied from ripple at $V_{OUT}$, through the feedback resistors as described in Options A and B below, or the ripple can be generated separately (using R5, C9, and C10) in order to keep the ripple at $V_{OUT}$ at a minimum (Option C).

**Option A) Lowest Cost Configuration:** In this configuration R4 is installed in series with the output capacitance (C7, C8). Since ≥25 mVp-p are required at the FB pin, R4 must be chosen to generate ≥50 mVp-p at $V_{OUT}$, knowing that the minimum ripple current in this circuit is ≅125 mAp-p at minimum $V_{IN}$. Using 0.43Ω for R4, the ripple at $V_{OUT}$ ranges from ≅54 mVp-p to ≅160 mVp-p over the input voltage range. If the application can accept this ripple level, this is the most economical solution. The circuit is shown in *Figure 2*. See *Figure 8*.

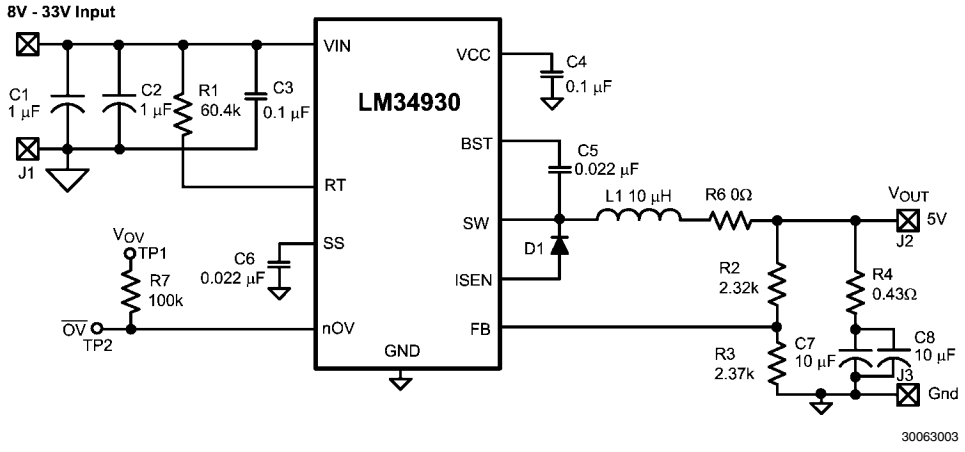



**FIGURE 2. Lowest Cost Configuration**

**Option B) Intermediate Ripple Configuration:** This evaluation board is supplied with this configuration installed. This configuration generates less ripple at $V_{OUT}$ than option A above by the addition of one capacitor (C11) across R2, as shown in *Figure 3*.

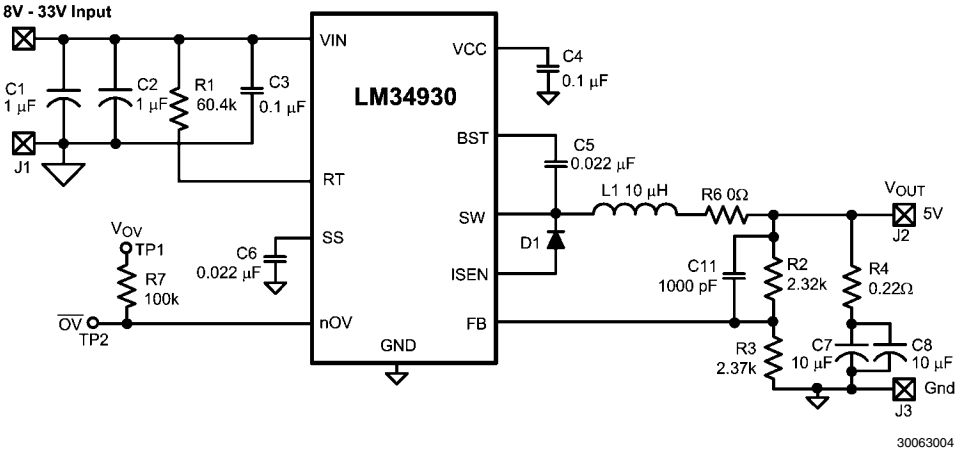



**FIGURE 3. Intermediate Ripple Configuration**

Since the output ripple is passed by Cff to the FB pin with little or no attenuation, R4 can be reduced so the minimum ripple at $V_{OUT}$ is ≅25 mVp-p. The minimum value for Cff is calculated from:

$$Cff \geq \frac{3 \times t_{ON\,(max)}}{(R2//R3)}$$

where $t_{ON(max)}$ is the maximum on-time (at minimum $V_{IN}$), and R2//R3 is the parallel equivalent of the feedback resistors. The ripple at $V_{OUT}$ ranges from 32 mVp-p to 93 mVp-p over the input voltagr range. See *Figure 8*.

**Option C) Minimum Ripple Configuration:** To obtain minimum ripple at $V_{OUT}$, R4 is set to 0Ω, and R5, C9, and C10 are added to generate the required ripple for the FB pin. In this configuration, the output ripple is determined primarily by the characteristics of the output capacitance and the inductor's ripple current. See *Figure 4*.

The ripple voltage required by the FB pin is generated by R5, C10, and C9 since the SW pin switches from -1V to $V_{IN}$, and the right end of C10 is a virtual ground. The values for R5 and C10 are chosen to generate a 50-100 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through C9. The following procedure is used to calculate values for R5, C10 and C9:

1) Calculate the voltage $V_A$:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN})))$$

where $V_{SW}$ is the absolute value of the voltage at the SW pin during the off-time (typically 1V), and $V_{IN}$ is the minimum input voltage. For this circuit, $V_A$ calculates to 4.63V. This is the approximate DC voltage at the R5/C10 junction, and is used in the next equation.

2) Calculate the R5 x C10 product:

$$R5 \times C10 = \frac{(V_{IN} - V_A) \times t_{ON}}{\Delta V}$$

where $t_{ON}$ is the maximum on-time (≅416 ns), $V_{IN}$ is the minimum input voltage, and ΔV is the desired ripple amplitude at the R5/C10 junction, 100 mVp-p for this example.

$$R5 \times C10 = \frac{(8V - 4.63V) \times 416\ ns}{0.1V} = 14 \times 10^{-6}$$

R5 and C10 are then chosen from standard value components to satisfy the above product. Typically C10 is 3000 to 10000 pF, and R5 is 10 kΩ to 300 kΩ. C9 is chosen large compared to C10, typically 0.1 µF. The ripple at $V_{OUT}$ is typically less than 10 mVp-p. See *Figure 4* and *Figure 8*.

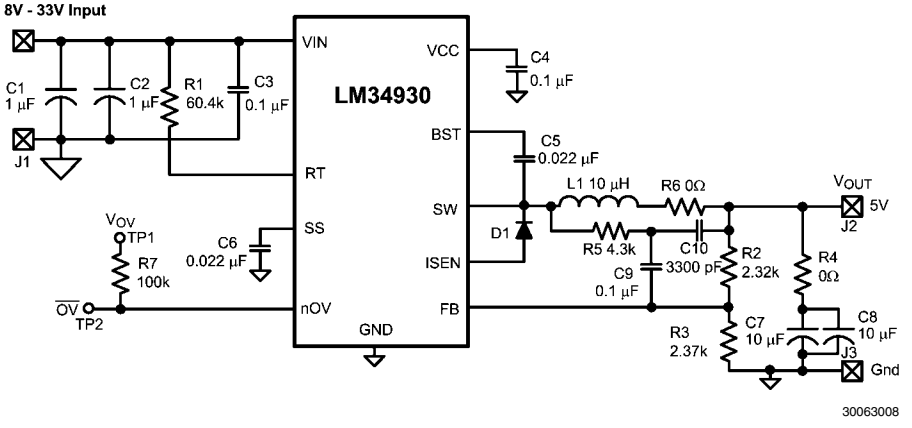



**FIGURE 4. Minimum Output Ripple Configuration**

## Over-Voltage Indicator

The nOV pin, an open drain logic output, switches low when the voltage at VIN exceeds 19V. The over-voltage indicator comparator provides 1.95V hysteresis to reject noise and ripple on the VIN pin. A pull-up voltage not exceeding 7V must be connected to TP1. A 100 kΩ pull-up resistor (R7) is provided on this board. The state of the nOV pin can be monitored at TP2.

The pull-up voltage can exceed the voltage at VIN. When nOV is low, the current into the pin must not exceed 10 mA.

## Input Over-Voltage Shutdown

If the input voltage at VIN increases above 36V an internal comparator disables the buck switch, and grounds the soft-start pin. The over-voltage shutdown comparator provides 400 mV hysteresis to reject noise and ripple on the VIN pin. Normal operation resumes when the voltage at VIN is reduced below the lower threshold.

## Monitor The Inductor Current

The inductor's current can be monitored or viewed on a scope with a current probe. Remove R6, and install an appropriate current loop across the two large pads where R6 was located. In this way the inductor's ripple current and peak current can be accurately determined.

## Scope Probe Adapters

Scope probe adapters are provided on this evaluation board for monitoring the waveform at the SW pin, and at the circuit's output ($V_{OUT}$), without using the probe's ground lead which can pick up noise from the switching waveforms. The probe adapters are suitable for Tektronix P6137 or similar probes, with a 0.135" diameter.

## Minimum Load Current

The LM34930 requires a minimum load current of ≅1 mA to ensure the boost capacitor (C5) is recharged sufficiently during each off-time. In this evaluation board, the minimum load current is provided by the feedback resistors allowing the board's minimum load current at $V_{OUT}$ to be specified at zero.

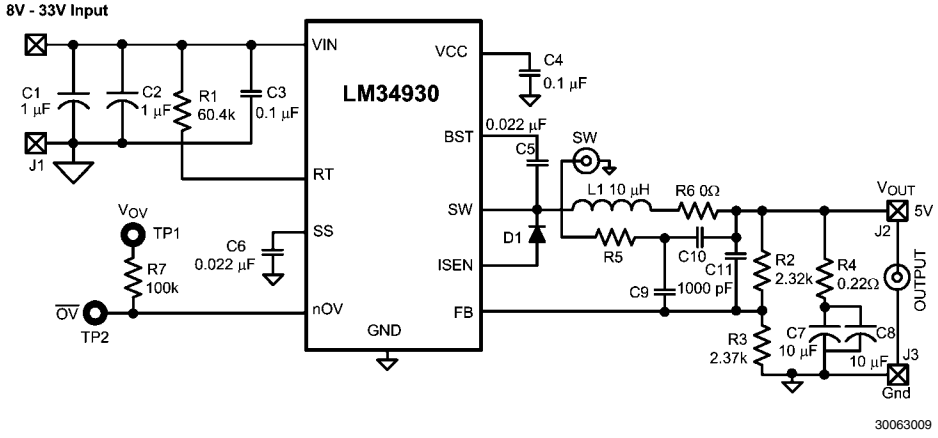



**FIGURE 5. Complete Evaluation Board Schematic (As Supplied)**

## Bill of Materials

| Item | Description | Mfg., Part Number | Package | Value |
|---|---|---|---|---|
| C1 | Ceramic Capacitor | TDK C3216X7R1H105M | 1206 | 1.0 µF, 50V |
| C2 | Ceramic Capacitor | TDK C3216X7R1H105M | 1206 | 1.0 µF, 50V |
| C3 | Ceramic Capacitor | TDK C1608X7R1H104K | 0603 | 0.1 µF, 50V |
| C4 | Ceramic Capacitor | TDK C1608X7R1H104K | 0603 | 0.1 µF, 50V |
| C5 | Ceramic Capacitor | TDK C1608X7R1H223K | 0603 | 0.022 µF, 50V |
| C6 | Ceramic Capacitor | TDK C1608X7R1H223K | 0603 | 0.022 µF, 50V |
| C7, C8 | Ceramic Capacitor | TDK C3216X7R1C106K | 1206 | 10 µF, 16V |
| C9 | Ceramic Capacitor | Unpopulated | 0603 | |
| C10 | Ceramic Capacitor | Unpopulated | 0603 | |
| C11 | Ceramic Capacitor | TDK C1608X7R2A102M | 0603 | 1000 pF |
| D1 | Schottky Diode | Zetex ZLLS2000 | SOT23-6 | 40V, 2.2A |
| L1 | Power Inductor | Bussman DR73-100 | 7.6 mm x 7.6 mm | 10 µH, 2A |
| R1 | Resistor | Vishay CRCW06036042F | 0603 | 60.4 kΩ |
| R2 | Resistor | Vishay CRCW06032321F | 0603 | 2.32 kΩ |
| R3 | Resistor | Vishay CRCW06032371F | 0603 | 2.37 kΩ |
| R4 | Resistor | Panasonic ERJ3RQFR22 | 0603 | 0.22Ω |
| R5 | Resistor | Unpopulated | 0603 | |
| R6 | Resistor | Vishay CRCW08050000Z | 0805 | 0Ω Jumper |
| R7 | Resistor | Vishay CRCW06031003F | 0603 | 100 kΩ |
| U1 | Switching Regulator | National Semiconductor LM34930TL | 12 Bump µSMD | |

## Circuit Performance

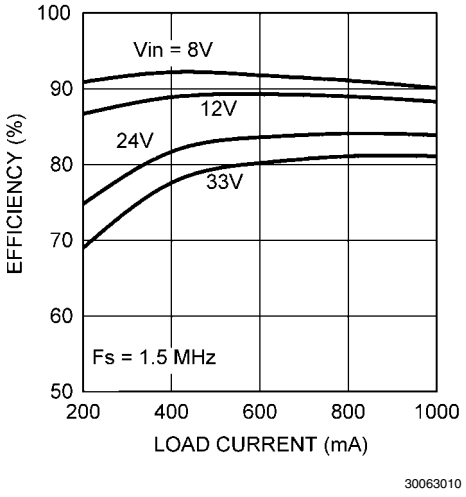



**FIGURE 6. Efficiency vs Load Current**

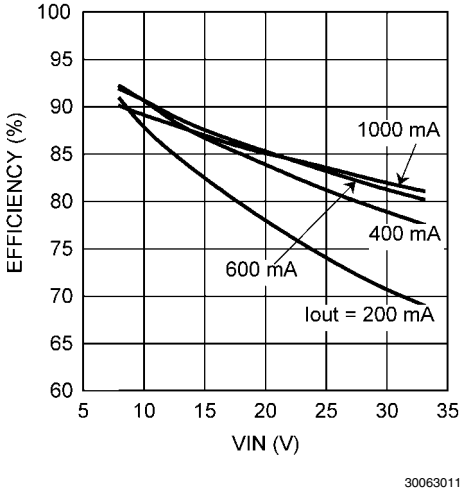



**FIGURE 7. Efficiency vs Input Voltage**

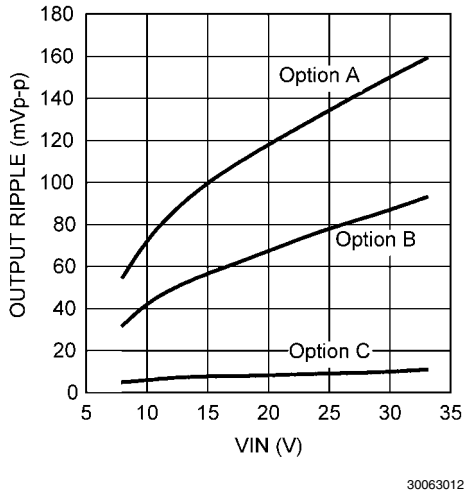



**FIGURE 8. Output Voltage Ripple**

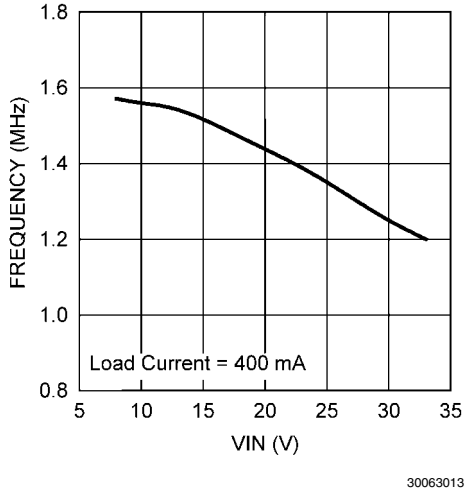



**FIGURE 9. Switching Frequency vs. Input Voltage**

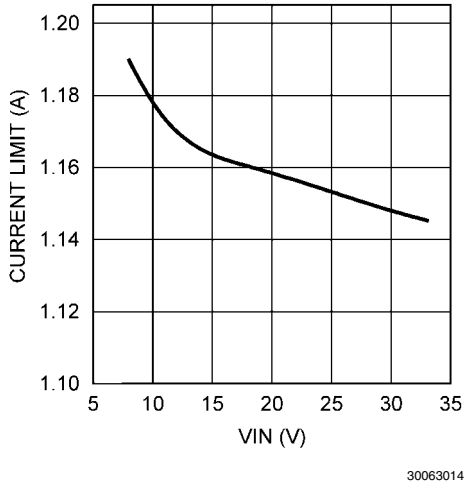
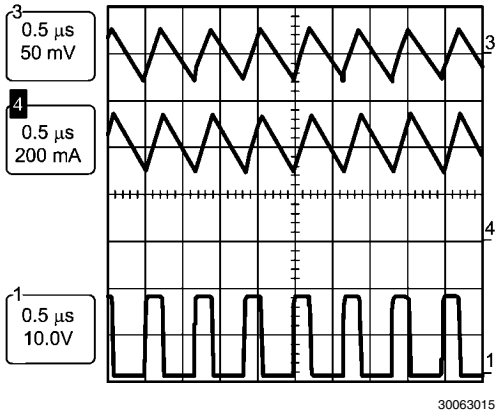


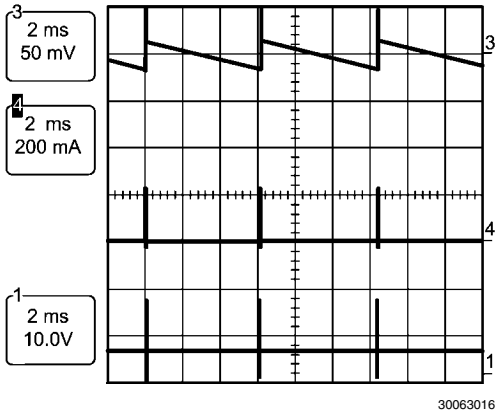

**FIGURE 10. Load Current Limit vs Input Voltage**

## Typical Waveforms




Trace 1 = SW Pin
Trace 3 = $V_{OUT}$
Trace 4 = Inductor Current
Vin = 16V, Iout = 400 mA

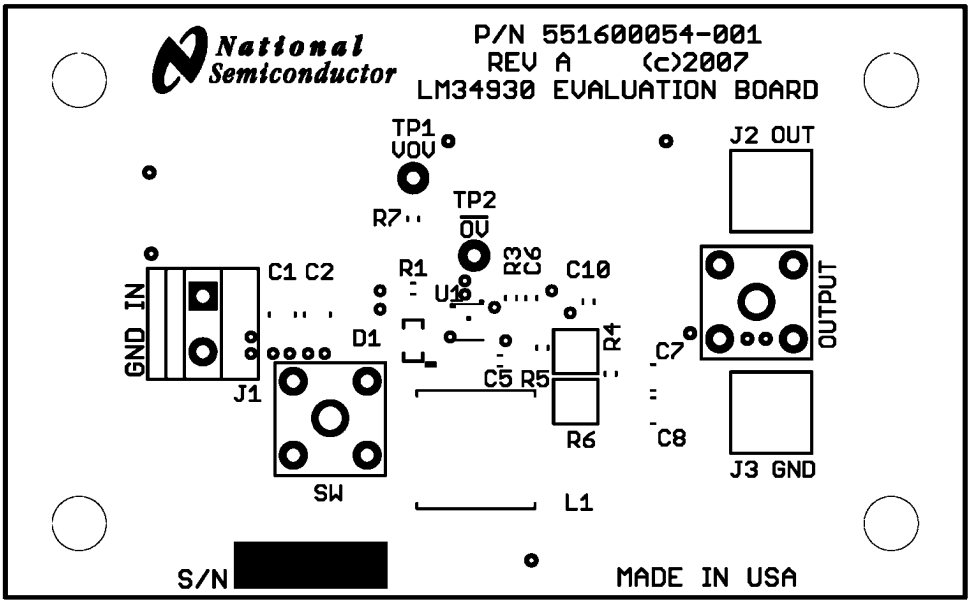
**FIGURE 11. Continuous Conduction Mode**




Trace 1 = SW Pin
Trace 3 = $V_{OUT}$
Trace 4 = Inductor Current
Vin = 16V, Iout = 0 mA

**FIGURE 12. Discontinuous Conduction Mode**

## PC Board Layout

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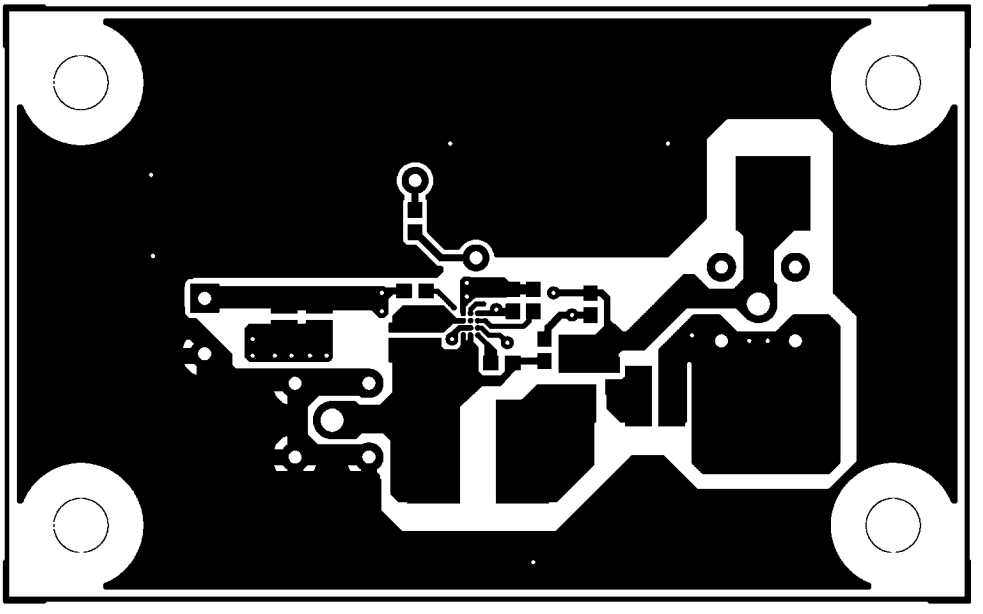
**Board Silkscreen**



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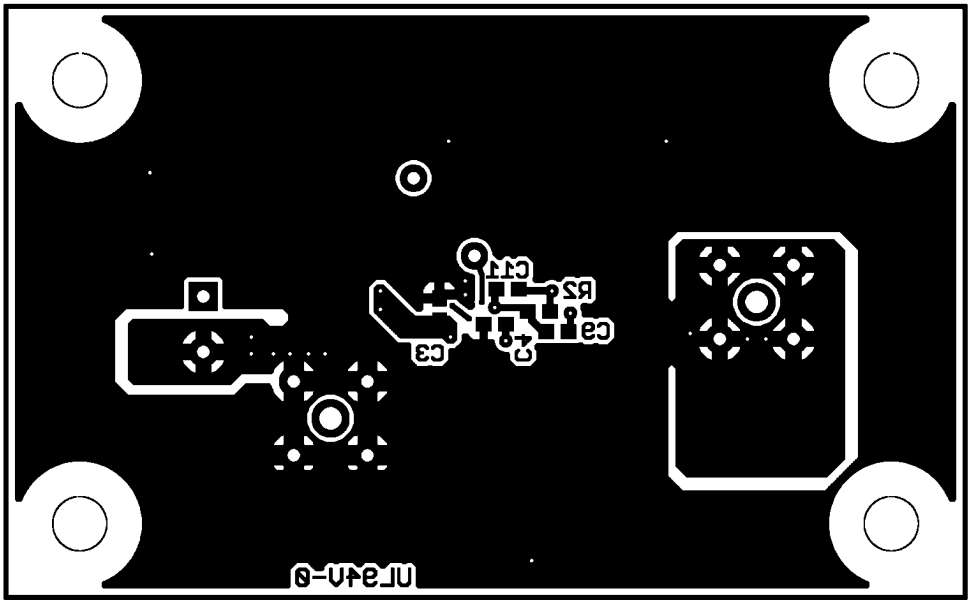
**Board Top Layer**

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**Board Bottom Layer (Viewed from Top)**

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